Patent Claims

1. An apparatus for executing a Viterbi algorithm,

- having a number of initial state registers, in each of which a state metric of an initial state of a trellis can be stored,
- having at least one transition register, in which a transition metric of the trellis can be stored,
- having an adder/subtracter network, which is connected to the initial state registers, to the transition register and to evaluation units in accordance with a butterfly structure of the trellis,
- having a number of evaluation units, in which the signals processed by the adder/subtracter network can be evaluated in accordance with the Viterbi algorithm,
- having a selection unit in which the apparatus can be switched between a first operating mode and a second operating mode,
- having a number of final state registers which are coupled to the evaluation units and in each of which a state metric of a respective final state of the trellis can be stored, and
- in which different evaluation units can be selected using the selection unit depending on the selected operating mode.

2. The apparatus as claimed in claim 1,
in which at least one of the initial state registers additionally has a buffer register.

3. The apparatus as claimed in claim 1 or 2,
which has at least one transition register for storing a transition metric when the apparatus is switched to the first operating mode, and/or for storing a change transition metric when the apparatus is switched to the second operating mode.

4. The apparatus as claimed in one of claims 1 to 3,
which has at least two transition registers for storing two different transition metrics, when the apparatus is switched to the second operating mode.

5. The apparatus as claimed in one of claims 1 to 4,
having a processor which is coupled to the registers by means of a signal bus.

6. The apparatus as claimed in claim 5,
in which the processor is designed for calculating the metrics.

7. The apparatus as claimed in one of claims 1 to 6,

having a memory which is coupled to the registers by means of a signal bus and in which the metrics can be stored.

8. The apparatus as claimed in one of claims 1 to 7, in which the adder/subtracter network has at least one adder and/or at least one subtracter.

9. The apparatus as claimed in claims 2 and 8, in which the adder/subtracter network has three adders and three subtracters, with

- a first input of a first adder being coupled to the output of a first transition register,
- a second input of the first adder being coupled to the output of a second transition register,
- a first input of a first subtracter being coupled to the output of the second transition register,
- a second input of the first subtracter being coupled to the output of a third transition register,
- a first input of a second adder being coupled to the output of the first buffer register,
- a second input of the second adder being coupled to the output of the first adder,
- a first input of a second subtracter being coupled to the output of the first buffer register,

- a second input of the second subtracter being coupled to the output of the first adder,
- a first input of a third adder being coupled to the output of the first subtracter,
- a second input of the third adder being coupled to the output of a second buffer register,
- a first input of a third subtracter being coupled to the output of the first subtracter, and
- a second input of the third subtracter being coupled to the output of the second buffer register.

10. The apparatus as claimed in one of claims 1 to 9, in which the evaluation units have

- a trace-back register, and/or
- comparison units, and/or
- maximum selection elements.

11. The apparatus as claimed in claim 10,

- in which a control input of a trace-back register is coupled to a control output of a first final state register in such a manner that, when a value is read from the first final state register, the trace-back register can store new values,
- in which a first data input of the trace-back register is coupled to the output of a first comparator, and

- in which a second data input of the trace-back register is coupled to the output of a second comparator.

12. The apparatus as claimed in claim 10 or 11,

- in which a first input of a first comparator is coupled to the output of the second adder,
- in which a second input of the first comparator is coupled to the output of the third subtracter,
- in which a first input of a second comparator is coupled to the output of the second subtracter, and
- in which a second input of the second comparator is coupled to the output of the third adder.

13. The apparatus as claimed in one of claims 10 to 12,

- in which a control input of first maximum selection element is coupled to the control output of the first final state register in such a manner that, when a value is read from the first final state register, the maximum selection element can select a new value,
- in which a first input of the first maximum selection element is coupled to the output of the second adder,
- in which a second input of the first maximum selection element is coupled to the output of the second subtracter,

- in which a control input of a second maximum selection element is coupled to a control output of the second final state register in such a manner that, when a value is read from the second final state register, the maximum selection element can select a new value,
- in which a first input of the second maximum selection element is coupled to the output of the third subtracter, and
- in which a second input of the second maximum selection element is coupled to the output of the third adder.

14. The apparatus as claimed in one of claims 1 to 13, in which the selection element has

- a selection register, and
- at least one multiplexer.

15. The apparatus as claimed in claim 14,

- in which the input of the selection register is coupled to the DSP bus,
- in which the output of the selection register is coupled to a control input of a first multiplexer,
- in which a first data input of the first multiplexer is coupled to a first data output of the trace-back register,

- in which a second data input of the first multiplexer is coupled to the output of the first maximum selection element,
- in which a control input of a second multiplexer is coupled to a second data output of the trace-back register,
- in which a first data input of the second multiplexer is coupled to the output of the second adder,
- in which a second data input of the second multiplexer is coupled to the output of the third subtracter,
- in which a control input of a third multiplexer is coupled to a third data output of the trace-back register,
- in which a first data input of the third multiplexer is coupled to the output of the second subtracter, and
- in which a second data input of the third multiplexer is coupled to the output of the third adder.

16. The apparatus as claimed in one of claims 1 to 15, in which the first operating mode is a mode in which decoding is carried out in accordance with the Viterbi algorithm.

17. The apparatus as claimed in one of claims 1 to 16,

in which the second operating mode is a mode in which equalization is carried out in accordance with the Viterbi algorithm.

18. A method for executing a Viterbi algorithm,

- in which a first operating mode or a second operating mode of an apparatus is selected in order to execute the Viterbi algorithm,
- in which a state metric of an initial state of a trellis is in each case stored in a respective initial state register,
- in which at least one transition metric of the trellis is stored, depending on the selected operating mode,
- in which the state metrics of the initial states and the transition metric are linked to one another in accordance with a butterfly structure of the trellis, in accordance with the Viterbi algorithm, depending on the selected operating mode,
- in which the linked variables are selected depending on the selected operating mode,
- in which the selected linked variables are stored as state metrics of a respective final state of the trellis, and
- in which the method is carried out iteratively until the Viterbi algorithm has been ended.

19. The method as claimed in claim 18,

used for processing physical signals.

20. The method as claimed in claim 19,

- in which the physical signals are decoded in the first operating mode, and
- in which the physical signals are equalized in the second operating mode.

21. The method as claimed in one of claims 18 to 20,

- in which, as soon as a final state has been read from a final state register, the respective state metric of the initial state of the trellis stored in the initial state register is in each case stored in a buffer register, and
- in which a new state metric of an initial state of a trellis is in each case stored in an initial state register as soon as the respective initial state of the trellis is stored in the buffer register.